IN THE SPECIFICATION

Please amend the specification as follows:

The paragraph beginning at page 15, line 18 is amended as follows:

During read, the ferroelectric write once read only memory cell, 301-1 or 301-2, is operated in the forward direction with the array plate 304 grounded and the bit line, 308-1 or 308-2, and respective second source/drain region or drain region, 306-1 and 306-2, of the cells precharged to some fractional voltage of VDD. If the device is addressed by the word line, 312-1 or 312-2, then the "imprint" of information stored in the ferroelectric capacitor dielectric will effect the conductivity of the transistor and will be detected using the sense amplifier 310. In one embodiment, the sense amplifier 310 utilizes an ENABLE signal as indicated in Figure 3. The operation of DRAM sense amplifiers is described, for example, in U.S. Pat. Nos. 5,627,785; 5,280,205; and 5,042,011, all assigned to Micron Technology Inc., and incorporated by reference herein. The array would thus be addressed and read in the conventional manner used in DRAM's, but programmed as write once read only memory cells in a novel fashion.